Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A buffer circuit comprising: operational amplification means which is configured to input an input voltage to a non-inverted input terminal and inputs an output voltage from an output terminal to an inverted input terminal through feedback; and output acceleration means which receives the input voltage and the output voltage as differential inputs and which outputs an electric current larger than a current output from the operational amplification means to the output terminal when a difference between the input voltage and the output voltage exceeds ~~exceeding~~ a predetermined offset voltage ~~exists between the differential inputs~~.

2. (Original) The buffer circuit according to claim 1, wherein the output acceleration means has a differential amplification section having the predetermined offset voltage, and a switching section which is connected between a source potential and the output terminal and is activated or deactivated in accordance with an output from the differential amplification section.

3. (Original) The buffer circuit according to claim 2, wherein the differential amplification section has a first differential amplification circuit which produces a first output when the input voltage is higher than the output voltage by an amount corresponding to a first offset voltage, and a second differential amplification circuit which produces a second output when the output voltage is higher than the input voltage by an amount corresponding to a second offset voltage; and wherein the switching section has a first switching circuit which is connected between a first source potential and the output terminal and is activated or deactivated in accordance with the first output, and a second switching circuit which is connected between the

output terminal and a second source potential and is activated or deactivated in accordance with the second output.

4. (Original) The buffer circuit according to claim 2, wherein the operational amplification means is formed such that an electric current output from a first source potential to the output terminal is limited to a predetermined current value and such that an electric current output from the output terminal to a second source potential flows by way of the switching circuit; and wherein the output acceleration means has a differential amplification section having the predetermined offset voltage and a switching section which is connected between the first source potential and the output terminal and is activated or deactivated in accordance with an output from the differential amplification section.

5. (Original) The buffer circuit according to claim 1, wherein said buffer circuit is used for at least any one of a plurality of buffer circuits which is used for a driver IC.

6. (Original) The buffer circuit according to claim 1, wherein said operational amplification means is an operational amplifier which includes a plurality of constant current sources.

7. (Previously Presented) A buffer circuit, comprising:

an input node and an output node;

an amplifier for driving said output node from a first power terminal when the voltage on said input node deviates from the voltage on said output node, said amplifier driving said output node at a first output current level to drive the output node to a voltage substantially equal to the voltage on the input node; and

an accelerator circuit for increasing the amount of current driven to the output node from the first power terminal when the voltage difference between the input terminal and the output terminal is above a predetermined delta voltage.